IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor	:	TAKANORI IWAMATSU, et al.
Reissue Application Of Patent No.	:	5,867,542
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Serial No.	:	08/552,543
Title	:	CLOCK PHASE DETECTING CIRCUIT AND CLOCK REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT
Examiner	:	Y. Tse
Group Art Unit	:	2614

January 26, 2001

BOX REISSUE
Assistant Commissioner for Patents
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Filed concurrently herewith is a reissue application of the above-referenced patent, including amended versions of all of the patent claims. Prior to examination on the merits, entry of this preliminary amendment is earnestly solicited.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Acct. No. 08-1634

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by Theresa Saunders

IN THE CLAIMS

Please add the following claims:

15. A receiver circuit arranged in a receiving unit of multiplex radio equipment, said receiving unit including an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal,an equalizing circuit for subjecting said demodulated signal to an equalizing process, and a clock regenerating circuit regenerating a signal identification clock for said identifying circuit and then supplying said signal identification clock to said identifying circuit; comprising:

a clock regenerating unit for regenerating said signal identification clock based on a signal before said multilevel orthogonal modulated signal is detected;

a phase adjusting unit for adjusting the phase of a clock from said clock regenerating unit and then supplying the phase-adjusted clock to said identifying circuit; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on

input/output signals of said equalizing circuit and then supplying the result as a phase adjustment control signal to said phase adjusting unit.

16. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit.

17. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and wherein said clock regenerating unit, said phase adjusting unit, and said clock phase detecting unit are used in common to said plural identifying units.

18. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, wherein said identifying circuit comprises plural

identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit; and wherein said clock regenerating unit, said phase adjusting unit, said averaging unit, and said clock phase detecting unit are used in common to said plural identifying units.

19. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and wherein said clock regenerating unit is shared among said plural identifying units; and wherein plural phase adjusting units and plural clock phase detecting units are arranged corresponding to said plural identifying units.

20. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15,

wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit; said clock regenerating unit is used in common to said plural identifying units; and a plurality of said phase adjusting units, said averaging units and said clock phase detecting units are arranged corresponding to said plural identifying units.

21. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, further comprising a test signal generating unit for generating a test signal; and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said test signal generating unit, said output of said selecting unit being supplied as an input to said phase adjusting unit.

22. A receiver circuit arranged in a receiving unit of multiplex radio equipment, said receiving unit including

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal,an equalizing circuit for subjecting said signal obtained by demodulating a multilevel orthogonal modulated signal and an equalizing circuit to an equalizing process, and a clock regenerating circuit regenerating a signal identification clock for said identifying circuit and then supplying said signal identification clock to said identifying circuit; comprising:

a clock phase detecting unit for detecting a phase component of said signal identification clock based on signals input to or output from said equalizing circuit;

a loop filter unit for integrating the output from said clock phase detecting unit; and

an oscillating unit for producing a signal identification clock for said identifying circuit to said identifying circuit, in response to as a control input the output from said loop filter unit.

23. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and wherein said clock phase detecting unit, said loop filter unit, and said oscillating unit are used in common to said plural identifying units.

24. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein plural clock phase detecting units are arranged to said identifying units; and wherein said loop filter unit and said oscillating unit are used in common to said identifying units; and further comprising a composing unit for composing the outputs of said clock phase detecting units to input the resultant output of said composing unit to said loop filter unit.

25. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising plural clock phase detecting units and plural loop filter units being arranged corresponding to said plural identifying units; said oscillating unit being used in common to said plural identifying units; a part of said plural identifying units being connected to said oscillating unit via said phase adjusting unit, said output of said loop filter unit being supplied as a control input to said oscillating unit or said phase adjusting unit.

26. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said plural identifying units; and further comprising a second clock phase detecting unit for detecting the phase component of said signal identification clock in a method different from that of said clock phase detecting unit and a composing unit for composing the output from said clock phase detecting unit with the output

from said second clock phase detecting unit, the output of said composing unit being supplied as an input to said loop filter unit.

27. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said plural identifying units; and further comprising a second clock phase detecting unit for detecting the phase component of said signal identification clock in a method different from that of said clock phase detecting unit and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said second clock phase detecting unit, the output of said selecting unit being supplied as an input to said loop filter unit.

28. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, further comprising a test signal generating unit for

generating a test signal; and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said test signal generating unit, said output of said selecting unit being supplied as an input to said loop filter unit.

29. A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said clock to said identifying circuit; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on clock phase difference information supplied to said identifying circuit and signal error differential information obtained by said identifying circuit and then supplying said resultant phase component to said clock regenerating circuit.

30. The receiver circuit arranged in a receiving unit

of multiplex radio equipment, according to claim 29,

wherein said clock phase detecting unit comprises:

a clock phase difference detecting unit for detecting said clock phase difference information supplied to said identifying circuit;

a signal error differential detecting unit for detecting signal error differential information obtained by said identifying circuit; and

a clock phase calculating unit for calculating the phase component of said signal identification clock based on the output from said clock phase difference detecting unit and the output from said signal error differential detecting unit.

31. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 29, wherein said clock phase calculating unit comprises a dividing unit that subjects the output of said error detecting unit and the output of said signal inclination detecting unit to a dividing calculation process.

32. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 29, wherein said clock phase calculating unit is formed as an

exclusive OR calculating unit that subjects the output of said error detecting unit and the output of said signal inclination detecting unit to an exclusive OR calculation process.

33. A receiver circuit arranged in a receiving unit of multiplex radio equipment, said receiving unit having an identifying circuit that identifies a signal obtained by demodulating a multilevel orthogonal modulated signal at a predetermined identification level, and a clock regenerating circuit regenerating a signal identification clock for said identifying circuit to supply said clock to said identifying circuit, comprising:

a clock regenerating unit for regenerating said signal identification clock based on a signal before said multilevel orthogonal modulation signal is detected;

a phase adjusting unit for adjusting the phase of a clock sent from said clock regenerating unit and supplying the resultant clock to said identifying circuit; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on clock phase difference information supplied to said identifying circuit and signal error differential information obtained by said identifying circuit and then

supplying said resultant phase component to said clock regenerating circuit.

34. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit.

35. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said clock regenerating unit, said phase adjusting unit, and said clock phase detecting unit are used in common to said plural identifying units.

36. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit; and wherein said clock regenerating unit, said phase adjusting unit, said averaging unit, and said clock phase detecting unit are used in common to said plural identifying units.

37. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said clock regenerating unit is used in common to said plural identifying units; and wherein plural phase adjusting units and plural clock phase detecting units are arranged corresponding to said plural identifying units.

38. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural

identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit; and wherein said clock regenerating unit is used in common to said plural identifying units, and a plurality of said phase adjusting units, said averaging units and said clock phase detecting units are arranged corresponding to said plural identifying units.

39. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, further comprising a test signal generating unit for generating a test signal; and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said test signal generating unit, said output of said selecting unit being supplied as an input to said phase adjusting unit.

40. A receiver circuit arranged in a receiving unit of multiplex radio equipment, said receiving unit including an identifying circuit for identifying a signal at a

predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal, and a clock regenerating circuit regenerating a signal identification clock for said identifying circuit and then supplying said signal identification clock to said identifying circuit; comprising:

a clock phase detecting unit for detecting a phase component of said signal identification clock based on clock phase difference information supplied to said identifying circuit and signal error differential information obtained by said identifying circuit and supplying said phase component to said clock regenerating circuit;

a loop filter unit for integrating the output from said clock phase detecting unit; and

an oscillating unit for producing a signal identification clock for said identifying circuit to said identifying circuit, in response to the output as a control input from said loop filter unit.

41. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and wherein said clock phase detecting unit, said loop filter unit, and said oscillating unit are used in common to said plural identifying units.

42. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said identifying units, and plural clock phase detecting units are arranged corresponding to said identifying units; and further comprising a composing unit that composes outputs of said plural clock phase detecting units and then supplies the resultant output as an input to said loop filter unit.

43. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising plural clock phase detecting units and plural loop filter units being arranged corresponding to said plural identifying units; said oscillating unit being used in common to said plural identifying units; a part of said plural identifying units being connected to said oscillating unit via said phase adjusting unit, said output of said loop filter unit being supplied as a control input to said oscillating unit or said phase adjusting unit.

44. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said plural identifying units; and further comprising a second clock phase detecting unit for detecting the phase component of said signal identification clock in a method different from that of said clock phase detecting unit and a composing unit for composing the output from said clock phase detecting unit with the output

from said second clock phase detecting unit, the output of said composing unit being supplied as an input to said loop filter unit.

45. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said plural identifying units; and further comprising a second clock phase detecting unit for detecting the phase component of said signal identification clock in a method different from that of said clock phase detecting unit and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said second clock phase detecting unit, the output of said selecting unit being supplied as an input to said loop filter unit.

46. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, further comprising a test signal generating unit for

generating a test signal; and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said test signal generating unit, said output of said selecting unit being supplied as an input to said loop filter unit.

47. A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and

a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase information to be supplied to said identifying circuit and signal error

information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,

said clock phase detecting section including

a difference detecting unit, responsive to the receipt of said composite input information, for detecting any one of (I) difference information between the demodulated signal and the equalized demodulated signal and (II) a combination of clock phase difference information and signal error differential information, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit.

REMARKS

The parent application, Serial No. 552, 543, filed November 3, 1995, was originally submitted with 46 claims. In the Examiner's first Office Action in the parent application, a restriction was required for examination of a single species of the invention from six species that were identified by the Examiner.

As a result of this restriction requirement, a first species, claims 1-14, directly related to Figure 1, was

elected. Claims 1-14 were subsequently allowed after amendment. Because no allowed claim was deemed generic, no additional species were examined at that time.

Subsequent review of the issued patent by the inventors led to the conclusion that an error had been made by reason of the patentees claiming less than they had the right to claim in the patent. In particular, the patentees concluded that a generic claim could have been included among the claims during prosecution of the elected species.

Had a generic claim been entered and allowed in the parent case, then following allowance of the elected claims, the Examiner would have examined a reasonable number of additional species. Failure to have additional species examined in the parent case was the penalty paid for the error of omitting a generic claim. The reissue application has the objective of rectifying that error and defining a generic claim and thereby also cover hopefully all species that were originally claimed in the parent application.

Therefore, in the presently filed reissue application, allowed claims 1-14 have been reintroduced with only the

slightest non-substantive modification as discussed hereinafter.

Claims 15-46 have been added. With only the slightest non-substantive changes, as discussed hereinafter, claims 15-46 in the reissue application are the same as claims 15-46 in the original parent application.

The Office Action of May 31, 1997, in the parent application, Serial No. 08/552,543, stated that the application contains claims directed to the following patentably distinct species of the claimed invention:

Claims 1-14 - directly related to Figure 1 of the first embodiment. Patent Col. 9, line 34 to Col. 11, line 48.

Claims 15-21 - directly related to Figure 2 of the second embodiment. Patent Col. 11, line 49 to Col. 14, line 8.

Claims 22-28 - directly related to Figure 3 of the third embodiment. Patent Col. 14, line 9 to Col. 16, line 21.

Claims 29-32 - directly related to Figure 4 of the fourth embodiment. Patent Col. 16, line 22 to Col. 17, line 26.

Claims 33-39 - directly related to Figure 5 of the fifth embodiment. Patent Col. 17, line 27 to Col. 19, line 40.

Claims 40-46 - directly related to Figure 6 of the sixth embodiment. Patent Col. 19, Line 41 to Col. 21, line 65.

Claim 47 has been added and is intended to relate to each of the six embodiments. The preamble to claim 47 states: "A receiver circuit arranged in a receiving unit of multiplex radio equipment ....."

Each of the other claims 1-46 has the identical opening language or has been amended to have the identical language to emphasize a generic relationship between the 47 claims. Thus, for example, allowed patent claim 1 is changed in the preamble from "A clock phase detecting circuit arranged in a receiving unit of multiplex radio equipment" to -- A receiver circuit arranged in a receiver unit of multiplex radio equipment--.

This is not a substantive change in the claim. It is clearly stated in the patent claim preamble that the clock phase detecting circuit is in a receiving unit of the radio equipment. Thus, now describing the invention in the claim preamble as a "receiver circuit in a receiving unit" is effected without a change of substance. Now, every claim has been amended to begin with, or already stated the same words. If the Examiner prefers, every claim could be amended to begin "A receiving unit of multiplex radio equipment…."

Because claims 15-46 were in the original application, clearly no new matter was added by reintroduction of those claims in the reissue application. Their relationships to the original disclosure has been indicated above where the six species are defined.

Claim 47 has been added. Claim 47 is a claim that was erroneously omitted from the parent application.

New claim 47 is comprised of features that were found in the original 46 claims and which are present in the claims 1-46 in prosecution here. New matter was not added in introducing claim 47.

The status of all claims 1-47, now in prosecution, is provided on a separate sheet annexed hereto.

Entry of this amendment and early examination of the reissue application on its merits is earnestly solicited.

Respectfully submitted,

Leonard Cooper 1/26/2001

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